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10/814,482	03/31/2004	Toshiharu Furukawa	ROC920030399US1	6082
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IBM CORPORATION ROCHESTER IP LAW DEPT. 917 3605 HIGHWAY 52 NORTH ROCHESTER, MN 55901-7829			EXAMINER GOODWIN, DAVID J	
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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/814,482  
Filing Date: March 31, 2004  
Appellant(s): FURUKAWA ET AL.

**MAILED**

**NOV 01 2007**

**GROUP 2800**

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William Allen  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 09/24/2007 appealing from the Office action mailed 07/11/2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

2003/0111699	Wasshuber
2004/0150042	Yeo

### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

#### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-11 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Wasshuber (US 2003/0111699).

3. Wasshuber teaches a semiconductor device. Said device comprises an island (525) of semiconductor material having a plurality of sidewalls and a strained region (paragraph 0031-0032) (fig 22). A handle wafer (514) and an insulating layer (512) disposed between said island (524) and said handle wafer (514). Said insulating layer (512) containing a thick region underlying the strained semiconductor island (524) and said insulating layer (512) electrically isolating said island (524) of said semiconductor material from said handle wafer (514). The underlying thickness of insulator insulating layer (512) exerts a tensile stress on the strained region (524) (paragraph 0042-0043) (fig 22).

4. Regarding claim 2.

5. Wasshuber teaches said insulating layer (512) comprises a buried oxide layer and said island is silicon (paragraph 0020-0021).
6. Regarding claim 3.
7. Wasshuber teaches a source (522a) and drain (522b) defined in the island (524), and a channel defined in the island between said source and said drain (fig 22) (paragraph 0034-0036). Said channel is disposed at least partially in said strained region of said island (fig 22) (paragraph 0042-0043).
8. Regarding claim 4.
9. Wasshuber teaches that the gate electrode (540) is isolated from said portion of the island (524) defining said channel (fig 22) (paragraph 0042-0043).
10. Regarding claim 5.
11. Wasshuber teaches that the insulating material (12b) divides the gate electrode (32) there being equal portions of the gate on each side of the midpoint of the straining layer(fig 1) (paragraph 0020-0022).
12. Regarding claim 6.
13. Wasshuber teaches that the gate electrode overlies the channel (fig 22).
14. Regarding claim 7.
15. Wasshuber teaches that that the structure comprises a semiconductor device (fig 22) (paragraph 000042-0043).
16. Regarding claim 8.
17. Wasshuber teaches that the island (524) comprises silicon and the thickened region of underlying insulator (512) comprises silicon dioxide (paragraph 0020-0021).

18. Regarding claim 9.

19. Wasshuber teaches that the underlying insulator comprises silicon dioxide (paragraph 0020-0021).

20. Regarding claim 10.

21. Wasshuber teaches that the wafer (514) comprises silicon and the thickness of underlying insulator (512) comprises silicon dioxide (paragraph 0020-0021).

22. Regarding claim 11.

23. Wasshuber teaches strained silicon enhances carrier mobility (paragraph 0003).

24. Regarding claim 13.

25. Wasshuber teaches the thickened region of said insulating layer (512) has a thickness greater than the surrounding insulating layer flanking said region, see the central portion of layer (512) and the ends of said layer (512) (fig 22).

26. Regarding claim 14.

27. Wasshuber teaches first and second anchors, comprising the portions of semiconductor overlying the ends of the thickened layer (512), flanking the strained region prevents relaxation of the strain region (fig 22).

28. Regarding claim 15.

29. Wasshuber teaches first and second anchors flanking, comprising the portions of semiconductor overlying the ends of the thickened layer (512), and adjacent to the strained region prevent relaxation of the strain region (fig 22).

30. Claims 1-4, 6-12, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo (US 2004/0150042).

31. Regarding claim 1

32. Yeo teaches a semiconductor device. Said device comprises an island (84) of semiconductor material having a plurality of sidewalls and a strained region (paragraph 0031-0032) (fig 30). A handle wafer (52) and an insulating layer (54) disposed between said island (84) and said handle wafer (52). Said insulating layer (54) containing a thick region underlying the strained semiconductor island (84) and said insulating layer electrically isolating said island (84) of said semiconductor material from said handle wafer (52). The underlying thickness of insulator exerts a tensile stress on the strained region (84) (paragraph 0031).

33. Regarding claim 2.

34. Yeo teaches said insulating layer (54) comprises a buried oxide layer and said island is silicon (paragraph 0031).

35. Regarding claim 3.

36. Yeo teaches a source defined in the island, a drain defined in the island, and a channel defined in the island between said source and said drain (fig 5) (paragraph 0034-0036). Said channel is disposed at least partially in said strained region of said island (fig 5).

37. Regarding claim 4.

38. Yeo teaches that the gate electrode is isolated from said portion of the island (84) defining said channel (fig 5) (paragraph 0036).

39. Regarding claim 6.

40. Yeo teaches that the gate electrode overlies the channel (fig 5).

41. Regarding claim 7.
42. Yeo teaches that that the structure comprises a semiconductor device (fig 5) (paragraph 0036).
43. Regarding claim 8.
44. Yeo teaches that the island comprises silicon and the thickness of underlying insulator comprises silicon dioxide (fig 0031).
45. Regarding claim 9.
46. Yeo teaches that the thickness of underlying insulator comprises silicon dioxide (fig 0031).
47. Regarding claim 10.
48. Yeo teaches that the wafer comprises silicon and the thickened region of underlying insulator comprises silicon dioxide (fig 0031).
49. Regarding claim 11.
50. Yeo teaches strained silicon enhances carrier mobility (0002).
51. Regarding claim 12.
52. Yeo teaches the thickness of oxide material (54) is more than 5 to 10 nanometers.
53. Regarding claim 14.
54. Yeo teaches first and second anchors, comprising the portions of semiconductor overlying the ends of the thickened layer (512), flanking the strained region prevent relaxation of the strain region (fig 5).
55. Regarding claim 15.



56. Yeo teaches first and second anchors, comprising the portions of semiconductor overlying the ends of the thickened layer (512), flanking and adjacent to the strained region prevent relaxation of the strain region (fig 5).

**(10) Response to Argument**

57. The appellant argues that Wasshuber fails to disclose an island of semiconductor material.

58. An island of semiconductor material is defined by bordering isolation regions (535a, 535b) (fig 22).

59. The appellant argues that Wasshuber does not teach an insulating layer disposed between the island and the handle wafer.

60. Wasshuber explicitly teaches that the silicon wafer (514) is implanted with oxygen in the region underlying the prospective device area (paragraph 0042). The implantation forms a region (512) which induces stress in the overlying region (paragraph 0043). Stress is induced by the implantation due to the impact of the implant on the lattice structure causing the volumetric expansion of the implanted region (paragraph 0021).

61. The impact of the implanted species on the lattice structure is the result of said species modifying and incorporating into the lattice. When oxygen incorporates and bonds with silicon atoms the result is silicon oxide, silicon oxide is an insulator.

62. The appellant argues that Wasshuber fails to disclose that any portion of the implanted region is thicker than any other portion of the implanted region.

63. This is a frivolous argument as the appellant does not, in claim 1, claim that any portion is thicker than any other portion. The appellant claims that the insulating layer comprises a thickened region.

64. Wasshuber clearly states that the implanted region has undergone a volumetric expansion (paragraph 0021) which necessarily requires an increase in the thickness. Further, as the appellant claims the structure rather than the method of making of a device, no patentable weight is accorded a process limitation such as thickening.

65. The appellant that Wasshuber discloses that the insulating layer (512) has the a uniform thickness across the entire width.

66. This is clearly a false statement. Wasshuber discloses in figure 22 that the implanted layer (512) comprises a central portion that is thicker than the end portions.

67. The appellant argues that Wasshuber fails to disclose that the insulating layer electrically isolates the island of semiconductor material due to gaps existing between the implanted region (512) and the isolation structures (535a, 535b).

68. The implanted region (512) forming an oxide will block the electrical currents the island of semiconductor material above the layer (512) from the handle wafer (below the layer (512)). That there may be some circuitous route which could conduct a small current around the isolating layer does not negate the isolation.

69. The appellant argues that Wasshuber does not detail the chemical reactions and processes to form a buried oxide layer.

70. The appellant does not claim such processes. Further, Wasshuber teaches that the substrate (514) reacts with the oxygen implant to form an expanded region (512).

This expansion will only take place if the oxygen reacts with the silicon which will form silicon oxide, an insulator. If as the appellant contends the oxygen does not react with the silicon than no expansion will take place which is counter to the teaching and intent disclosed by Wasshuber.

71. The appellant argues that Wasshuber discloses a uniformly thickened silicon layer not a an insulating layer having one portion thicker than abother.

72. Wasshuber discloses that a region of the substrate undergoes expansion as a result of an oxygen implantation (paragraph 0033). To undego expansion the lattice structure must be changed, when this structural change is caused by oxygen the change is the transformation of silicon lattice to a silicon oxide lattice.

73. Further, the appellant does not claim that one portion is thicker than another protion. The appellant claims that the layer is thickened.

74. Wasshuber clearly discloses that the layer has undergone an expansion, is thickened. Also Wasshuber clearly discloses that the central portion of the implanted region (512) is thicker than the peripheral portions (fig 22).

75. The appellant argues that the thickening differential is *de facto* set forth in claim 1.

76. Such a limitation is clearly not set forth in claim 1.

77. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

78. Claim 1 recites that a thickened region underlies the island, the claim does not claim or suggest that there is any differential in the thickness. The appellant claims a differential in the thickness of the insulating layer in claim 13 not claim 1.

79. Said differential in thickness is disclosed in Wasshuber layer (512) (fig 22).

80. The appellant argues Yeo fails to disclose a thickened region underlying the strained region.

81. That an underlying layer is thickened comprises a process limitation in that a layer undergoes an expansion to be thickened.

82. A "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in *Thorpe*,

a. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*. 411 F2d 1345, 1348, 162 USPQ 145, 147, (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir 1935).

83. Yeo teaches an insulating layer (54) that has a thickness underlying the strained region (84). Whether or not said layer was thinner at sometime in the past does not lend patentable weight to the device claim.

84. The appellant argues that Yeo does not teach that the insulating layer (54) transfers stress to the strained layer (56).

85. Yeo teaches that the insulating layer transfers stress to the strained layer (paragraph 0031). If the underlying layer did not stress the overlying layer the overlying layer would not be strained. Without stress from the underlying layer, the overlying layer would relax (i.e. not be strained).

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

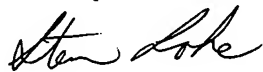
David Goodwin

Conferee:

Ricky Mack



Steven Loke



David Goodwin

